ABSTRACT

A method is presented comprising analyzing two or more input terms on a per-bit basis within each level of bit-significance. Maximally segmenting each of the levels of bit-significance into one or more one-, two-, and/or three-bit groups, and designing a hyperpipelined hybrid Wallace tree adder utilizing one or more full-adders, half-adders, and associated register based, at least in part, on the maximal segmentation of the input terms.